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10/525,203	02/22/2005	Yuichi Takagi	SON-2815	7661

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EXAMINER	
JOSEPH, DENNIS P	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/525,203	TAKAGI ET AL.	
	Examiner	Art Unit	
	DENNIS P. JOSEPH	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2005* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/28/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to application No. 10/525203 on Febuary 25, 2005.

Claims 1-28 are pending and have been examined.

Information Disclosure Statement

2. The information disclosure statement (IDS) was submitted on January 28. 2008 has been

received and is been considered by the examiner.

Claim Rejections – 35 USC § 103

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 103(a) that forms the basis for the rejections under this section made in this Office action:
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:
1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. **Claims 1-28** rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi

(6,332,661) in view of Koyama et al. (7,180,496 B2)

Yamaguchi teaches in Claim 1:

A current output type drive circuit for outputting a drive current to a driven object shared by being divided into a plurality of areas (Figure 1 shows the current drivers used to drive the EL devices 51, 52, etc (read as a plurality of areas)),

comprising a plurality of drivers arranged corresponding to each the shared area of the driven object (Figure 1, driver ICS 1, 2 and 3, Column 5, Lines 41-46),

each driver comprising

an output means for outputting a supplied reference current and the drive current corresponding to image data to a corresponding shared area of the driven object (Figure 1, output terminals 001-064, Column 5, Lines 41-46. The terminals output the current from the driver circuits to the pixel elements), and

a reference current source circuit (Figure 1, reference current generation circuit 12); but

However, Yamaguchi does not explicitly teach the reference current source circuit is used "for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means."

However, in the same field of endeavor, display devices with sampling circuits, Koyama teaches of a circuit including shift register circuits 201 in which sampling pulses are outputted to latch circuits 202 in which they are respectively held therein. (Koyama, Figure 2 shows 201 and 202 and the resulting signal is then sent to the pixels 205. Column 9, Lines 15-25). The circuits together from 201 to 205 can be interpreted as a sampling and holding circuit which takes an

input, processes it and outputs it through the use of memory circuits (as shown in Figure 4) to the pixel.

Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to integrate the sampling and holding circuitry within Yamaguchi's reference current generation circuit with the motivation that by using the circuits and processing the signal in this manner, it will result in reducing power consumption while the display can still be displayed in high quality. (Koyama, Column 2, Lines 32-57)

Yamaguchi and and Koyama teach in Claim 2:

A current output type drive circuit as set forth in claim 1, wherein said reference current source circuit (Yamaguchi, Figure 1, reference current generation circuit 12) comprises at least:

a current sampling circuit (The combination with Koyama teaches to use the sampling circuits including 201-205) including a current memory for sampling and holding said reference current in accordance with a control signal (Koyama, Column 16, Lines 13-18 disclose memory circuits used to store the held and sampled signals) and

a control circuit for outputting to said current sampling circuit a control signal for controlling write and read operations of said reference current of the current memory of said current sampling circuit. (Koyama, Column 16, Lines 13-18 disclose writing to the volatile memory and also outputting signals using the memory circuits as well as volatile/non-volatile memories. Columns 8-9, Lines 57-3)

Koyama teaches in Claim 3:

A current output type drive circuit as set forth in claim 2, wherein

said current sampling circuit includes a first current memory and a second current memory (Column 11, Lines 36-43, first current memory comprises A1 to A3 or B1 to B3 as shown in Figure 4 and the second current memory comprises C1 to C3), and

said control circuit outputs to said current sampling circuit said control signal so as to alternately perform a write operation of the reference current input from said reference current input terminal and a read operation of the written reference current on said first current memory and second current memory. (Column 11, Lines 36-43, storing and write operations (read as reading and writing of signals), storing to A1 to A3 or B1 to B3 and writing to C1 to C3)

Yamaguchi and Koyama teaches in Claim 4:

A current output type drive circuit as set forth in claim 2, wherein said output means

includes a plurality of current output type digital/analog conversion circuits (Koyama, Figure 14 shows D/A circuits 1404. These are commonly used in the art) and the circuit comprises means for increasing the reference current read from the current memory of the current sampling circuit of said reference current source circuit to a plurality of reference currents by further copying or distributing them by time division, and said plurality of reference currents are supplied to said plurality of digital/analog conversion circuits. (The combination with Yamaguchi teaches to use the reference current generation circuit 12 as shown in Figure 1 to distribute the plurality of reference currents to each of the current drivers and these are done over a time period which is also common in the art, Koyama, Column 10, Lines 1-21)

Yamaguchi and Koyama teach in Claim 5:

A current output type drive circuit as set forth in claim 4, wherein

each driver is a driver outputting currents of a plurality of channels in accordance with input data (Figure 1 shows the output of the respective constant current drivers),

further comprises a register array for holding said input data (Figure 2 shows register 70 within IC driver 1, Column 6, Lines 46-52) and

further comprises means for increasing the reference current sampled and held by the reference current source circuit to a plurality of reference currents by further copying or distributing them by time division (The combination with Yamaguchi teaches to use the reference current generation circuit 12 as shown in Figure 1 to distribute the plurality of reference currents to each of the current drivers and these are done over a time period which is also common in the art, Koyama, Column 10, Lines 1-21), and

said output means comprises

a plurality of conversion circuits for receiving said plurality of reference currents (Koyama, Figure 14 shows D/A circuits 1404. These are commonly used in the art) and outputting currents in accordance with the data held by the register array (Figure 2 shows the data being sent to the output terminals 001 to 064) and

a current output circuit comprising a first group of current sampling circuits and a second group of current sampling circuits operating alternately in a current write mode and current read mode in accordance with the output currents of the conversion circuits. (The combination with Koyama teaches to use the multiple current memories, Column 11, Lines 36-43, first current

memory comprises A1 to A3 or B1 to B3 as shown in Figure 4 and the second current memory comprises C1 to C3)

Yamaguchi and Koyama teach in Claim 6:

A current output type drive circuit as set forth in claim 5, wherein

said input data is digital image data (Koyama, Colu mn 2, Lines 57-60),

the circuit comprises means for distributing the reference current to the drivers in a vertical blanking period during which operations on said image data are suspended (Yamaguchi, Figure 1 shows the enable signal for turning on/off the operation while the reference current generation circuit distributes the reference current to the drivers), and

each driver uses as the reference current the current held in the reference current source circuit of the driver after the vertical blanking period in which digital noise is generated along with transfer of said image data. (Figure 1 shows the circuit 12 sending out signals with small variations which are produced as reference signals, Yamaguchi Columns 2-3, Lines 45-14)

Yamaguchi teaches in Claim 7:

A current output type drive circuit for outputting a drive current to a driven object shared by being divided into a plurality of areas (Figure 1 shows the current drivers used to drive the EL devices 51, 52, etc (read as a plurality of areas)),

comprising a plurality of drivers arranged corresponding to each the shared area of the driven object (Figure 1, driver ICS 1, 2 and 3, Column 5, Lines 41-46),

each driver comprising

an output means for outputting a supplied reference current as a drive current to the corresponding shared area of the driven object (Figure 1, output terminals 001-064, Column 5, Lines 41-46. The terminals output the current from the driver circuits to the pixel elements) and

a reference current source circuit (Figure 1, reference current generation circuit 12)

the reference current input terminal being connected to a reference current input terminal of another driver by a common current interconnect (Figure 1, the reference current generation circuit 12 branches and inputs to each of the drivers, which achieves the same result as if it was a common line to each); but

However, Yamaguchi does not explicitly teach the reference current source circuit is used "for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means." Furthermore, while he does not explicitly teach "the reference current being distributed to the reference current source circuits of the drivers-by time division."

However, in the same field of endeavor, display devices with sampling circuits, Koyama teaches of a circuit including shift register circuits 201 in which sampling pulses are outputted to latch circuits 202 in which they are respectively held therein. (Koyama, Figure 2 shows 201 and 202 and the resulting signal is then sent to the pixels 205. Column 9, Lines 15-25). The circuits together from 201 to 205 can be interpreted as a sampling and holding circuit which takes an input, processes it and outputs it through the use of memory circuits (as shown in Figure 4) to

the pixel. Furthermore, Koyama, Column 10, Lines 1-21 discloses it being done in a time divided manner with periods and this is common in the art.

Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to integrate the sampling and holding circuitry within Yamaguchi's reference current generation circuit with the motivation that by using the circuits and processing the signal in this manner, it will result in reducing power consumption while the display can still be displayed in high quality. (Koyama, Column 2, Lines 32-57)

Yamaguchi teaches in Claim 8:

A current output type drive circuit as set forth in claim 7, wherein each driver fetches said reference current from said reference current input terminal to said reference current source circuit when receiving a signal indicating start of distribution of the reference current and outputs the signal indicating the start of distribution of reference current to the driver circuit of the next stage. (Figure 1, control circuit 11 for on-off controlling of the driving current in correspondence with an input signal, Column 5, Lines 39-50)

Yamaguchi and Koyama teach in Claim 9:

A current output type drive circuit as set forth in claim 8, wherein each driver comprises a data memory, writes input data into said data memory when receiving a first signal indicating start of writing of data and outputs said first signal indicating start of writing of data to the driver of the next stage and fetches said reference current from said reference current input terminal to

said reference current source circuit in synchronization with said first signal when receiving a second signal indicating start of distribution of reference current and outputs said second signal indicating start of distribution of reference current to the driver circuit of the next stage. (The combination with Koyama teaches to use the memory circuits to read and write the signals in conjunction with Yamaguchi's reference current generation circuit and to output them to the pixels)

Yamaguchi and Koyama teach in Claim 10:

A current output type drive circuit as set forth in claim 7, wherein said reference current source circuit (Yamaguchi, Figure 1, reference current generation circuit 12) comprises at least:

a current sampling circuit (The combination with Koyama teaches to use the sampling circuits including 201-205) including a current memory for sampling and holding said reference current in accordance with a control signal (Koyama, Column 16, Lines 13-18 disclose memory circuits used to store the held and sampled signals) and

a control circuit for outputting to said current sampling circuit a control signal for controlling write and read operations of said reference current of the current memory of said current sampling circuit. (Koyama, Column 16, Lines 13-18 disclose writing to the volatile memory and also outputting signals using the memory circuits as well as volatile/non-volatile memories. Columns 8-9, Lines 57-3)

Koyama teaches in Claim 11:

A current output type drive circuit as set forth in claim 10, wherein

said current sampling circuit includes a first current memory and a second current memory (Column 11, Lines 36-43, first current memory comprises A1 to A3 or B1 to B3 as shown in Figure 4 and the second current memory comprises C1 to C3), and

said control circuit outputs to said current sampling circuit said control signal so as to alternately perform a write operation of the reference current input from said reference current input terminal and a read operation of the written reference current on said first current memory and second current memory. (Column 11, Lines 36-43, storing and write operations (read as reading and writing of signals), storing to A1 to A3 or B1 to B3 and writing to C1 to C3)

Yamaguchi and Koyama teaches in Claim 12:

A current output type drive circuit as set forth in claim 10, wherein said output means includes a plurality of current output type digital/analog conversion circuits (Koyama, Figure 14 shows D/A circuits 1404. These are commonly used in the art) and

the circuit comprises means for increasing the reference current read from the current memory of the current sampling circuit of said reference current source circuit to a plurality of reference currents by further copying or distributing them by time division, and said plurality of reference currents are supplied to said plurality of digital/analog conversion circuits. (The combination with Yamaguchi teaches to use the reference current generation circuit 12 as shown in Figure 1 to distribute the plurality of reference currents to each of the current drivers and these are done over a time period which is also common in the art, Koyama, Column 10, Lines 1-21)

Yamaguchi teaches in Claim 13:

A current output type drive circuit as set forth in claim 7, wherein at least the reference current source circuit of the driver serving as a master includes a reference current source circuit generating a reference current and supplying it to said common current interconnect. (Figure 1 shows the reference current generation circuit 12 acting as a 'master' circuit by applying current to each of the drivers)

Yamaguchi teaches in Claim 14:

A current output type drive circuit as set forth in claim 10, wherein at least the reference current source circuit of the driver serving as a master includes a reference current source circuit generating a reference current and supplying it to said common current interconnect. (Figure 1 shows the reference current generation circuit 12 acting as a 'master' circuit by applying current to each of the drivers)

Yamaguchi and Koyama teach in Claim 15:

A current output type drive circuit as set forth in claim 7, wherein

each driver is a driver outputting currents of a plurality of channels in accordance with input data (Figure 1 shows the output of the respective constant current drivers),

further comprises a register array for holding said input data (Figure 2 shows register 70 within IC driver 1, Column 6, Lines 46-52), and

further comprises means for increasing the reference current sampled and held by the reference current source circuit to a plurality of reference currents by further copying or

distributing them by time division (The combination with Yamaguchi teaches to use the reference current generation circuit 12 as shown in Figure 1 to distribute the plurality of reference currents to each of the current drivers and these are done over a time period which is also common in the art, Koyama, Column 10, Lines 1-21), and

said output means comprises

a plurality of conversion circuits for receiving said plurality of reference currents (Koyama, Figure 14 shows D/A circuits 1404. These are commonly used in the art) and outputting currents in accordance with the data held by the register array (Figure 2 shows the data being sent to the output terminals 001 to 064) and

a current output circuit having a first group of current sampling circuits and a second group of current sampling circuits operating alternately in a current write mode and current read mode in accordance with the output currents of the conversion circuits. (The combination with Koyama teaches to use the multiple current memories, Column 11, Lines 36-43, first current memory comprises A1 to A3 or B1 to B3 as shown in Figure 4 and the second current memory comprises C1 to C3)

Yamaguchi and Koyama teach in Claim 16:

A current output type drive circuit as set forth in claim 15, wherein

said input data is digital image data (Koyama, Column 2, Lines 57-60),

the circuit comprises means for distributing the reference current to the drivers in a vertical blanking period during which operations on said image data are suspended (Yamaguchi,

Figure 1 shows the enable signal for turning on/off the operation while the reference current generation circuit distributes the reference current to the drivers), and

each driver uses as the reference current the current held in the reference current source circuit of the driver after the vertical blanking period in which digital noise is generated along with transfer of said image data. (Figure 1 shows the circuit 12 sending out signals with small variations which are produced as reference signals, Yamaguchi Columns 2-3, Lines 45-14)

Yamaguchi teaches in Claim 17:

A current output type drive circuit as set forth in claim 7, wherein the interconnect of said reference current is arranged between power supply interconnects for shield. (Figure 1 shows the interconnect lines in between each driver and the power supply Vcc as shown in Figure 3. Column 7, Lines 12-24. The structure of the interconnect is the same and the shielding, or insulating structure is well known in the art and Examiner takes Official Notice as to the use of insulating layers used to shield the drivers)

Yamaguchi teaches in Claim 18:

A current output type drive circuit as set forth in claim 7, wherein the interconnect of said reference current, when a multilayer interconnect including a power supply layer for shield, is arranged at a top layer of said power supply layer for shield. (Figure 1 of Yamaguchi shows the interconnect and the use of insulating layers is well known in the art)

Yamaguchi teaches in Claim 19:

A current output type drive circuit as set forth in claim 7, further comprising means for suppressing great fluctuations of the potential of said common reference current interconnect when the circuits sampling and holding the reference currents of the drivers are all off. (Figure 1 shows the control circuits for on-off controlling of the driving current in correspondence with an input signal, Column 5, Lines 39-50. When off, there would obviously be a suppression of potential)

Yamaguchi teaches in Claim 20:

A current output type drive circuit as set forth in claim 12, wherein

said means increasing said reference current to a plurality of reference currents comprises a current mirror circuit configured by a constant current source (Column 6, Lines 57-63, current mirror circuit 120 from a constant current driver circuit 10) including resistor elements arranged at the input stage and a plurality of reference current sources including resistor elements arranged at the output stage in parallel so as to correspond to the output parts of said output means (Figure 1 shows the plurality of sources arranged in parallel to the output terminals. Column 5, Lines 57-65 disclose of a reference resistance which is mounted on the drivers and includes the current drivers), and

the resistor elements of the reference current sources arranged at the two ends among said plurality of reference current sources are arranged close to the resistor elements of said constant current source. (Column 5, Lines 57-65 disclose resistances 13 which is wired to each of the drivers, thus affecting them)

Yamaguchi teaches in Claim 21:

A current output type drive circuit as set forth in claim 20, wherein the resistor elements forming the reference current sources are laid out divided and cross-laced. (Figure 1, Column 5, Lines 57-65 shows the resistance 13 to be 'divided' and wired to each of the drivers for the intended effect)

Yamaguchi teaches in Claim 22:

A display device for outputting a drive current to a shared area of a display panel shared by being divided into a plurality of areas (Figure 1 shows the current drivers used to drive the EL devices 51, 52, etc (read as a plurality of areas)),

comprising a plurality of drivers arranged corresponding to each the shared area of the display panel (Figure 1, driver ICS 1, 2 and 3, Column 5, Lines 41-46),

each driver comprising an output means for outputting a supplied reference current to a corresponding shared area of the driven object (Figure 1, output terminals 001-064, Column 5, Lines 41-46. The terminals output the current from the driver circuits to the pixel elements) and

a reference current source circuit (Figure 1, reference current generation circuit 12)

However, Yamaguchi does not explicitly teach the reference current source circuit is used "for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means."

However, in the same field of endeavor, display devices with sampling circuits, Koyama teaches of a circuit including shift register circuits 201 in which sampling pulses are outputted to latch circuits 202 in which they are respectively held therein. (Koyama, Figure 2 shows 201 and 202 and the resulting signal is then sent to the pixels 205. Column 9, Lines 15-25). The circuits together from 201 to 205 can be interpreted as a sampling and holding circuit which takes an input, processes it and outputs it through the use of memory circuits (as shown in Figure 4) to the pixel.

Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to integrate the sampling and holding circuitry within Yamaguchi's reference current generation circuit with the motivation that by using the circuits and processing the signal in this manner, it will result in reducing power consumption while the display can still be displayed in high quality. (Koyama, Column 2, Lines 32-57)

Yamaguchi teaches in Claim 23:

A display device for outputting a drive current to a shared area of a display panel shared by being divided into a plurality of areas (Figure 1 shows the current drivers used to drive the EL devices 51, 52, etc (read as a plurality of areas)),

comprising a plurality of drivers arranged corresponding to each the shared area of the display panel (Figure 1, driver ICS 1, 2 and 3, Column 5, Lines 41-46),

each driver comprising

an output means for outputting a supplied reference current to a corresponding shared area of the driven object (Figure 1, output terminals 001-064, Column 5, Lines 41-46. The terminals output the current from the driver circuits to the pixel elements) and

a reference current source circuit (Figure 1, reference current generation circuit 12)

the reference current input terminal being connected to a reference current input terminal of another driver by a common current interconnect (Figure 1, the reference current generation circuit 12 branches and inputs to each of the drivers, which achieves the same result as if it was a common line to each); but

However, in the same field of endeavor, display devices with sampling circuits, Koyama teaches of a circuit including shift register circuits 201 in which sampling pulses are outputted to latch circuits 202 in which they are respectively held therein. (Koyama, Figure 2 shows 201 and 202 and the resulting signal is then sent to the pixels 205. Column 9, Lines 15-25). The circuits together from 201 to 205 can be interpreted as a sampling and holding circuit which takes an input, processes it and outputs it through the use of memory circuits (as shown in Figure 4) to the pixel. Furthermore, Koyama, Column 10, Lines 1-21 discloses it being done in a time divided manner with periods and this is common in the art.

Therefore, it would have been obvious to a person with ordinary skill in the art at the time of the invention to integrate the sampling and holding circuitry within Yamaguchi's reference current generation circuit with the motivation that by using the circuits and processing the signal in this

manner, it will result in reducing power consumption while the display can still be displayed in high quality. (Koyama, Column 2, Lines 32-57)

Yamaguchi teaches in Claim 24:

A display device as set forth in claim 23, wherein each driver fetches said reference current from said reference current input terminal to said reference current source circuit when receiving a signal indicating start of distribution of reference current and outputs the signal indicating start of distribution of reference current to the driver circuit of the next stage. (Figure 1, control circuit 11 for on-off controlling of the driving current in correspondence with an input signal, Column 5, Lines 39-50)

Yamaguchi and Koyama teach in Claim 25:

A display device as set forth in claim 23, wherein each driver comprises a data memory, writes input data into said data memory when receiving a first signal indicating start of writing of data and outputs said first signal indicating start of writing of data to the driver of the next stage and fetches said reference current from said reference current input terminal to said reference current source circuit in synchronization with said first signal when receiving a second signal indicating start of distribution of reference current and outputs said second signal indicating start of distribution of reference current to the driver circuit of the next stage. (The combination with Koyama teaches to use the memory circuits to read and write the signals in conjunction with Yamaguchi's reference current generation circuit and to output them to the pixels)

Yamaguchi teaches in Claim 26:

A display device as set forth in claim 23, wherein the interconnect of said reference current is arranged between power supply interconnects for shield. (Figure 1 shows the interconnect lines in between each driver and the power supply Vcc as shown in Figure 3. Column 7, Lines 12-24. The structure of the interconnect is the same and the shielding, or insulating structure is well known in the art and Examiner takes Official Notice as to the use of insulating layers used to shield the drivers)

Yamaguchi teaches in Claim 27:

display device as set forth in claim 23, wherein the interconnect of said reference current, when a multilayer interconnect including a power supply layer for shield, is arranged at a top layer of said power supply layer for shield. (Figure 1 of Yamaguchi shows the interconnect and the use of insulating layers is well known in the art)

Yamaguchi teaches in Claim 28:

A display device as set forth in claim 23, further comprising means for suppressing great fluctuations of the potential of said common reference current interconnect when the circuits sampling and holding the reference currents of the drivers are all off. (Figure 1 shows the control circuits for on-off controlling of the driving current in correspondence with an input signal, Column 5, Lines 39-50. When off, there would obviously be a suppression of potential)

Response to Arguments

5. Applicant's arguments considered, but are respectively not persuasive.

Applicant argues that the Yamaguchi and Koyama references cannot be combined because Koyama teaches of voltage signals which are sampled and held. However, the combination is important to note here as Yamaguchi does indeed teach of a reference current generation source, identical to Applicant's reference current source circuit. Please take note of the similar structure and functionality of Applicant's Figure 4 and Yamaguchi's Figure 1. Yamaguchi does indeed of the current source means, this much is not argued by Applicant. However, all he is lacking is a means to sample and hold his current data. While a sample and hold circuit is obvious in its use in circuits, Koyama was combined nonetheless to teach of a means for sampling and holding. The fact that Koyama's is done for voltage does not teach away, nor does it make the combination with Yamaguchi unreasonable since the primary reference explicitly teaches of a current source means. Both current and voltage application means are common in the art with several types of displays. Furthermore, Yamaguchi even teaches of a latch and register in Figure 2, similar to what Koyama teaches. This further reinforces that these two references can be indeed be combined. Again, Yamaguchi teaches of the current source means, just not of a means to sample and hold a signal, which is common in the art to do so, for current and voltage signals.

Applicant argues that the Office Action does not teach of separate current memories for use in storing, analyzing and outputting the signal. However, Koyama does teach various times throughout his disclosure of these memory circuits. They are circuits which perform the same claimed limitations of Applicant's, so the functionality is the same. As for Applicant's assertion

that the memories do not perform the read and write operations as claimed, Column 11, Lines 36-43 and Column 14, Lines 50-53 disclose of the alternating read/write for the memory circuits.

Applicant argues that there is no teaching of a vertical blanking period. However, Yamaguchi teaches in Column 6, Lines 22-45 of sending various clock signals to control the displayed information. This is used in conjunction with the current memories of reading and more importantly, writing information to the display. These would inherently include means to blank the display as well as writing desired information to it. This is controlled by the various signals as shown in Figure 1.

The Examiner took Official Notice in the first action in response to a claimed limitation for a shield. In the Remarks, the Applicant wishes to have references cited to support this notice. From Applicant's specification and with knowledge of one with ordinary skill in the art, this is taken to be an insulating structure around the various components. Applicant has not disputed the interpretation on this; it is rather common in the art to use these shielding means. The Examiner lists below several references which utilize these shield layers or shielding means in a display system:

Makishima et al. (US 2002/0075218 A1) - ([0184], [0262])

Yamazaki et al. (US 2002/0011975 A1) - ([0147)

Kikkawa (US 2001/0043184 A1) - ([0011])

Yasukawa (US 2001/0043175 A1) - ([0014])

Miyawaki et al. (US 2001/0040549 A1) - ([0160], [0172])

Again, Applicant's arguments considered, but are respectively not persuasive.

Conclusions

6. Applicant's arguments were respectively considered non-persuasive. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis P. Joseph whose telephone number is 571-270-1459. The examiner can normally be reached on Monday-Friday, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJ

/Amare Mengistu/

Supervisory Patent Examiner, Art Unit 2629